# 4.2K MULTICHANNEL READOUT CIRCUITRY IN A STANDARD 0.7μm PROCESS FOR A PHOTOCONDUCTOR ARRAY

Ybe Creten, Patrick Merken, Jan Putzeys, Chris Van Hoof
IMEC, MCP-DET, Kapeldreef 75, 3001 Heverlee, Belgium

## ABSTRACT

With the increasing performance of infrared sensors (i.e. dark current, QE, noise), the performance of the analog read-out electronics becomes more and more a determining factor in the overall system performance. For low temperature readout circuits, dedicated architectures and design techniques are needed rather than a translation of uncooled circuitry by trial and error. In this paper we present the cryogenic design and performance of a cold CMOS multichannel readout circuit to be used for the Ge:Ga focal plane detectors in the Photoconductor Array Camera and Spectrometer (PACS) aboard the Herschel Space Observatory. Key issues in the design of this 18-channel readout are noise, bias stability, linearity and low power consumption. As the specifications in this project are tighter than in our previous cryogenic designs for ISOPHOT, the use of robust architectures and design techniques is essential.
Both simulations and cryogenic tests show an amplifier open loop gain above 2000, a non-linearity error below 2 % over a dynamic output range of more than 2 V and an input-referred noise spectral density of less than 200 nV/$\sqrt{Hz}$ at 30 Hz for a total power consumption of 100 μW for the 18 channels.

## INTRODUCTION

The cryogenic design and performance of a cold CMOS multichannel readout circuit to be used for the Ge:Ga focal plane detectors in the Photoconductor Array Camera and Spectrometer (PACS) aboard the Herschel Space Observatory (formally known as FIRST) is presented. These detectors are arranged in a 25 by 16 matrix and will be cooled down to 1.5 K. In this configuration, 25 low-power multichannel read-outs (CRE: Cold Read-out Electronics) are required.
This paper summarizes the design, implementation and test results of such a CRE.

## DESIGN DETAILS

### Overview

The complete cold readout electronics chip (CRE) consists of 18 channels (unit cells), 16 connected to the focal plane detectors and 2 diagnostic channels, one open and one connected to a dummy resistor. The digital control signals, reset, sample and multiplex, are generated by digital logic, consisting of digital cells from a previously developed cryogenic library [1].

The unit cells are critical as they determine the performance of the CRE (Figure 1). Cryogenic design (<30 K) tended to be empirical and typically used dedicated “cryo”-technologies[2], but progress has been made in the recent years. For better portability and scalability of this design, a standard 0.7 μm CMOS process is used. In addition, robust architectures and design techniques were developed and circuits were successfully designed using a commercial circuit simulator (SpectreS) with experimentally extracted transistor model parameters.

*Contact information for Y.Creten: Email: creten@imec.be, phone (32) 16 288 168*

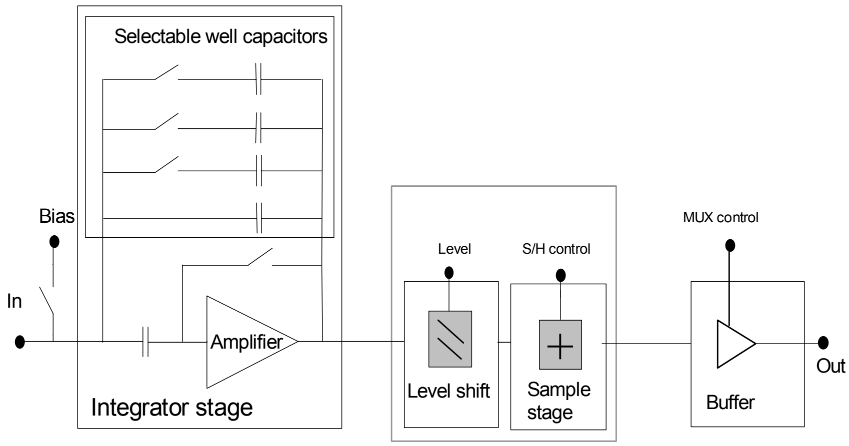



***Figure 1 :*** *architecture of a unit cell*

## Unit cell

The complete unit cell architecture is a self-biasing AC coupled Capacitive Transimpedance Amplifier (SAC), a sample and hold stage and an output driver. The Capacitive Transimpedance Input Amplifier (CTIA) structure used in this design consists of a very high gain amplifier, four selectable integrating capacitors in feedback to accommodate for the different backgrounds, a reset switch over the capacitors and a decoupling capacitor. By using this Self-biasing AC Coupled circuit (SAC) [3] rather than a conventional CTIA used in non-cryogenic readouts, the output is not influenced by the trip point drifts of the amplifiers and an excellent bias stability can be achieved. The most critical building block of such a SAC is the low power, high gain (>1000) amplifier. Until now, it had been believed that such high gains were hard to achieve because of the anomalous behavior of MOS transistors below 30 K. The topology selected to achieve this specification in this particular 4.2 K-project is a cascode pmos amplifier. This choice was made because the behavior of the pmos transistor at these low temperature is less prone to cryogenic anomalities[4]. The cascode allows to keep the nmos transistor out of the 'kink' region ($V_{DS}$<2 V).

A buffered sample-and-hold stage provides isolation between the sensible input stage and the sampling capacitor. This allows to read out a final point on a slope while already resetting the CTIA stage, without losing the linearity in the first part of the next slope (Figure 2).

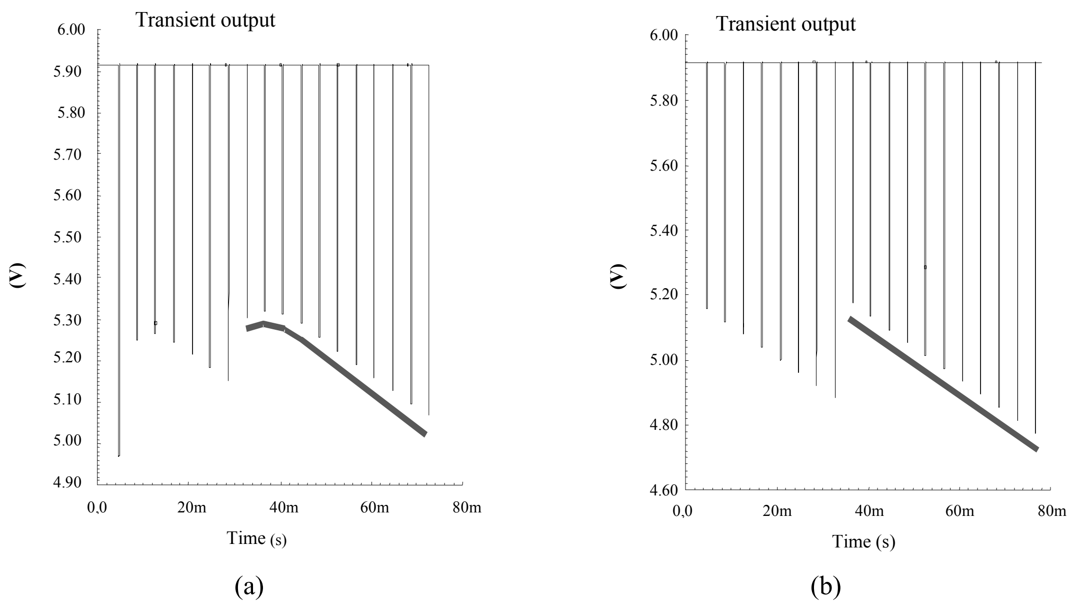



***Figure 2 :*** Sampled output of the CRE with a) conventional sample and hold stage and b) buffered sample and hold stage

The buffered sample and hold as well as the output buffer are pmos based structures to minimize the influence of cryogenic effects on linearity. However, a drawback of this approach is the signal shift typical caused by the amplifiers. A level shift circuit in front of the sample and hold stage nullifies the signal shift and ensures the required output dynamic range of >2 V (Figure 3).

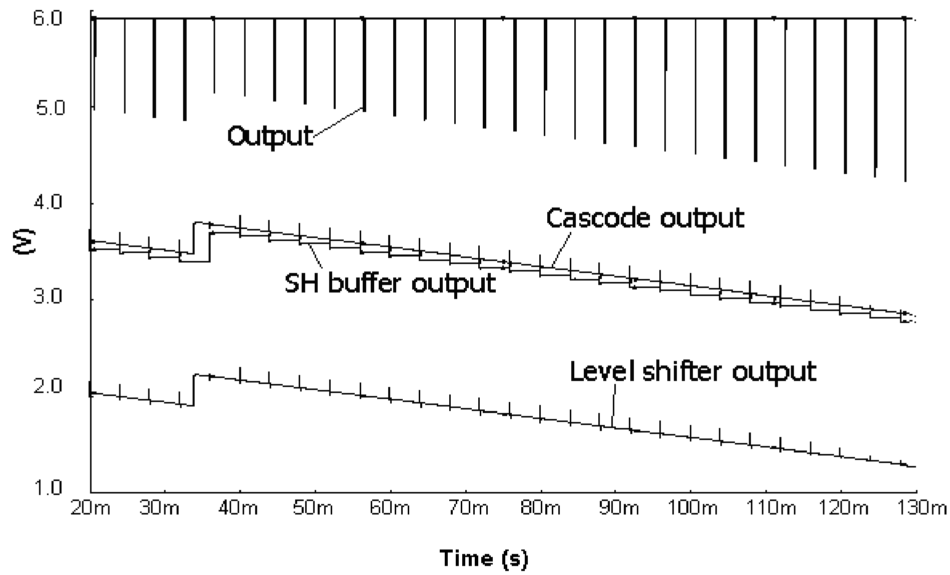



***Figure 3 :*** Signal levels in analog readout channel (simulation results)

## IMPLEMENTATION AND TEST RESULTS

The architectures discussed in the previous paragraphs are implemented in the Alcatel Mietec standard 0.7 µm CMOS process. Figure 4 shows the global assembly of the CRE die and passive elements on the alumina substrate.

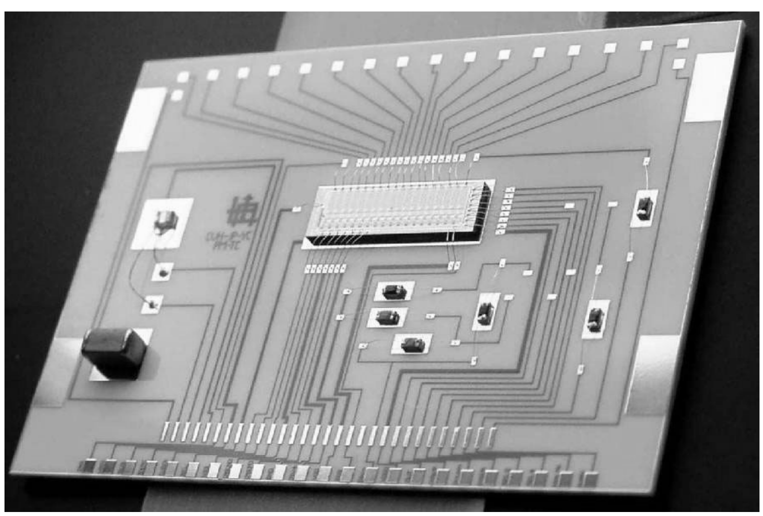


***Figure 4:*** CRE assembly for PACS instrument

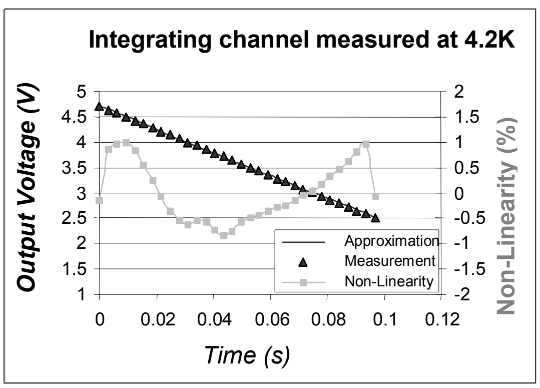
Room temperature as well as cryogenic measurements are performed on both the chip and the assembly. The experimental results, summarized in the table below, are in good agreement with the simulations on the circuit by the commercial circuit simulator (SpectreS).

***Table 1*** *: measurement results at 4.2 K*

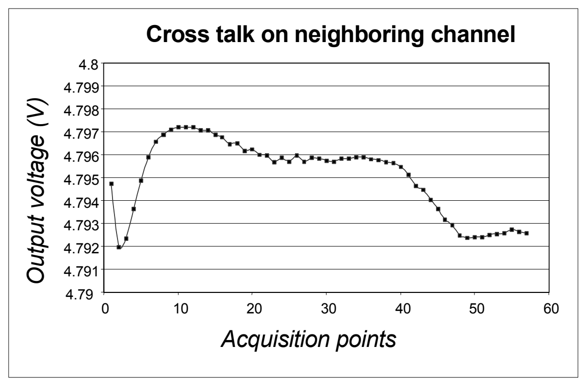
| | |
|---|---|
| *Dynamic Output range* | *>2 V* |
| *Detector debiasing* | *<1 mV over full dynamic range* |
| *Non-linearity error* | *<2 % over full dynamic range* |
| *Power consumption (18 channels)* | *100 $\mu W$* |
| *Cross talk* | *<2 %* |
| *Input referred noise of the amplifier* | *<200 nV/$\sqrt{Hz}$ at 30 Hz* |

As the open loop gain of the amplifier in the SAC structure is more than 2000, a detector debiasing of less than 1 mV is achieved over the full 2 V dynamic output range. The input referred noise of the amplifier is <200 nV/$\sqrt{Hz}$ at 30 Hz as predicted by simulations.

The non-linearity error on an integration ramp is below 2 % (Figure 5), while the cross talk measured on neighboring channels is lower than 2 %. The power consumption is 100 µW for the complete CRE (18 channels). As the input stage is only biased with 500nA, the greater part of the total power consumption is used in the output buffer.




(a)




(b)

***Figure 5:*** *a)* Integration ramp (left scale) and associated non-linearity error (right scale) and b) Cross talk on neighboring channel

# CONCLUSION

A design for an 18-channel cryogenic readout electronics chip for Ge:Ga infrared detectors on the PACS instrument has been presented and the major parts of the circuit are described. Measurements on both chip and assembly at low temperatures show that the design goals for this application have been met.

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# REFERENCES

1. B.Dierickx, Ph.D. dissertation, K.U.Leuven (Belgium), 1999.
2. R Glidden, S. Lizotte, J. Cable, L. Mason and C. Cao, “Optimization of cryogenic CMOS processes for sub-10K applications”, Proc. SPIE, Vol. 1684, pp.2-39,1992.
3. Previous work on 4K electronics done at IMEC and published in : O. Charlier, T. Cronje, C. A. Van Hoof, “Cryogenic standard CMOS sensor read-out electronics”, Proc. of SPIE, Vol. 4131, 2000 and internal research reports (1999).
4. E. Simoen, B. Dierickx, C. Claeys, “Analytical Model for the Kink in nMOST’s operating at liquid Helium Temperatures (LHT)”, Solid State Electronics, Vol. 33, pp.445- 454, 1990.